DATA SHEET

CGY2032BTS
DECT 500 mW power amplifier

Product specification
Supersedes data of 2000 Mar 14
File under Integrated Circuits, IC17

2000 Aug 22

Philips
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DECT 500 mW power amplifier CGY2032BTS

FEATURES

- Power Amplifier (PA) overall efficiency 55%
- 27.5 dBm saturated output power at 3.2 V
- 0 dBm input power
- 40 dB linear gain
- Operation without negative supply
- Wide operating temperature range –30 to +85 °C
- SSOP16 package.

APPLICATIONS

- 1.88 to 1.9 GHz transceivers for DECT applications
- 2 GHz transceivers: Personal Handy phone System (PHS), Digital Cellular System (DCS) and Personal Communication Services (PCS).

GENERAL DESCRIPTION

The CGY2032BTS is a GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate from 3.6 V battery supply.
No negative supply voltage is required for operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER(1)	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	3.2	–	V
I_{DD}	total drain current	–	350	–	mA
P_o	output power	–	27.5	–	dBm
T_{amb}	ambient temperature	–30	–	+85	°C

Note

1. For conditions, see Chapters “AC characteristics” and “DC characteristics”.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2032BTS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM

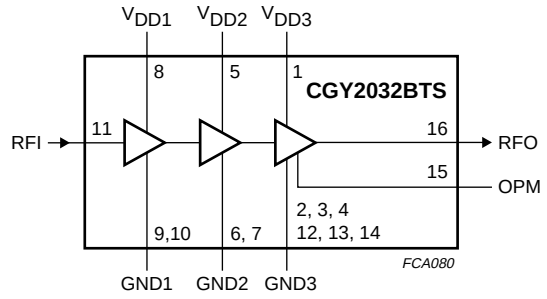


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD3}	1	third stage supply voltage
GND3	2	third stage ground supply
GND3	3	third stage ground supply
GND3	4	third stage ground supply
V_{DD2}	5	second stage supply voltage
GND2	6	second stage ground supply
GND2	7	second stage ground supply
V_{DD1}	8	first stage supply voltage
GND1	9	first stage ground supply
GND1	10	first stage ground supply
RFI	11	PA input
GND3	12	third stage ground supply
GND3	13	third stage ground supply
GND3	14	third stage ground supply
OPM	15	output pre-matching
RFO	16	PA output

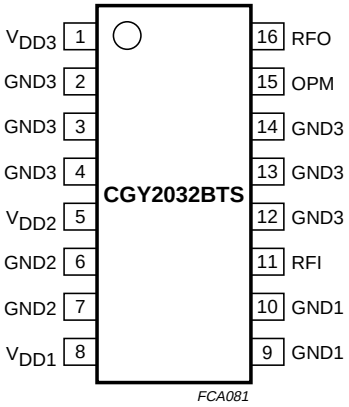


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Amplifier

The CGY2032BTS is a 3-stage GaAs power amplifier capable of delivering 500 mW (typical value) at 1.9 GHz into a 50 Ω load. Each amplifier stage has an open-drain configuration. The drains have to be loaded externally by adequate reactive circuits which must also provide a DC path to the supply.

The amplifier can be switched off by means of a single external PNP or PMOS series switch connected between the battery and the amplifier drains.

This switch can also be used to vary the actual supply voltage applied to the amplifier and hence, control the output power.

This device is specifically designed to work with a duty factor of 50% and can work up to 100% with good thermal performance printed-circuit boards.

Biasing

Internal biasing is provided inside the amplifier for class AB operation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	operating supply voltage	note 1	–	5.2	V
$T_{j(max)}$	maximum operating junction temperature		–	150	°C
P_{tot}	total power dissipation	note 2	–	450	mW
P_i	input power		–	15	dBm
T_{stg}	storage temperature		–55	+125	°C

Notes

1. On Philips evaluation board.
2. On Philips evaluation board; P_{tot} = 600 mW (maximum value).

HANDLING

Do not operate or store near strong electrostatic fields. Meets class 1 ESD test requirements of Human Body Model (HBM) in accordance with *"MIL STD 883C - method 3015"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	145	K/W

Note

1. On Philips evaluation board; $R_{th(j-a)}$ = 80 K/W (typical value).

DC CHARACTERISTICS

T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins V_{DD1}, V_{DD2} and V_{DD3}						
V_{DD}	positive supply voltage		1.8	3.2	4.2	V
I_{DD0}	positive peak supply current	V_{DD} = 3.2 V	–	–	800	mA

AC CHARACTERISTICS

V_{DD} = 3.2 V; f_{RF} = 1900 MHz; P_i = 0 dBm; T_{amb} = 25 °C; duty factor δ = 50%; 50 Ω impedance system; measured and guaranteed on the CGY2032BTS evaluation board; circuit diagram shown in Fig.5.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_i	input power		–5	0	+5	dBm
δ	duty factor		–	50	100	%
P_o	output power	V_{DD} = 3.2 V	26.5	27.5	29	dBm
		V_{DD} = 2.2 V	24	25	27	dBm
I_{DD}	total drain current	V_{DD} = 3.2 V	–	350	500	mA
		V_{DD} = 2.2 V	–	–	400	mA
η	efficiency		–	55	–	%
P_{leak}	RF leakage to output in power off state	V_{DD} = 0 V	–	–40	–35	dBm
H2	second harmonic level		–	–	–30	dBc
H3	third harmonic level		–	–	–35	dBc
Stab	stability (spurious levels)	note 1	–	–60	–	dBc

Note

1. The device is adjusted to provide nominal load power into a 50 Ω load. The device is switched off and a 3 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 3 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

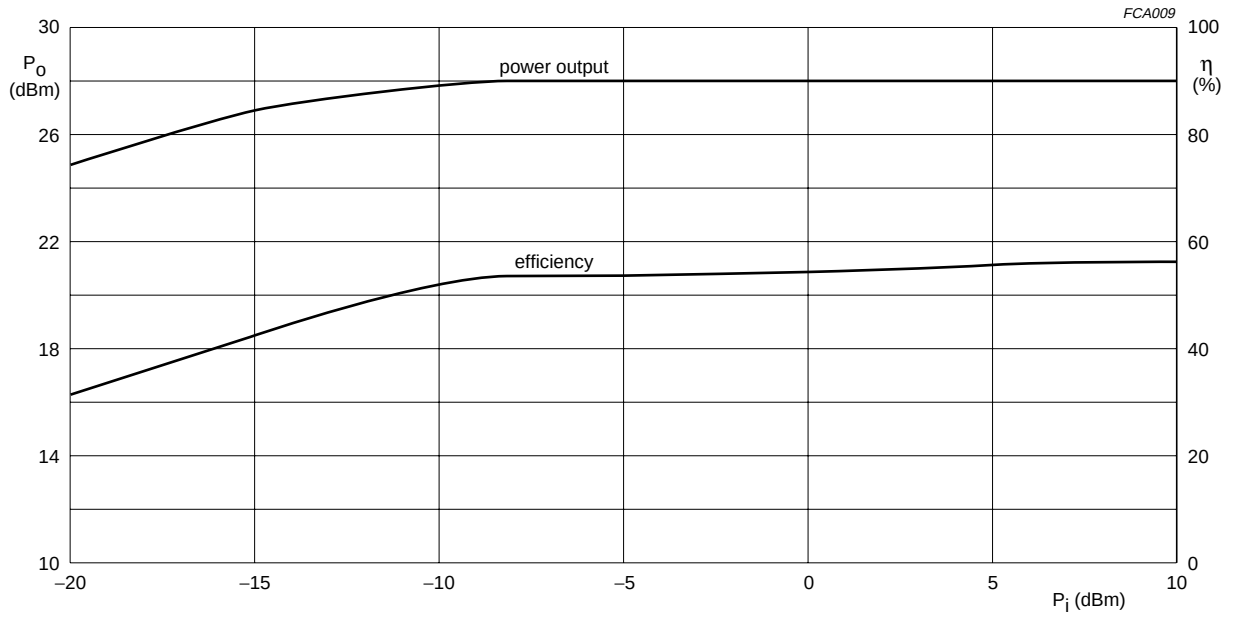


Fig.3 Typical output power and efficiency as a function of input power at V_{DD} = 3.2 V.

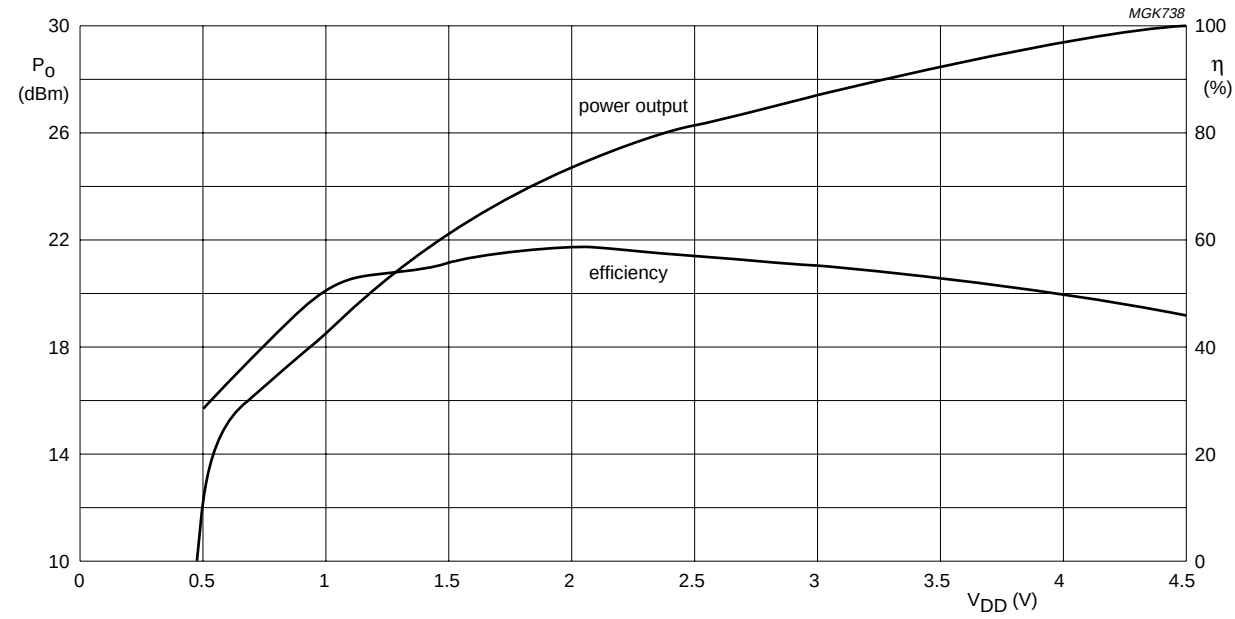
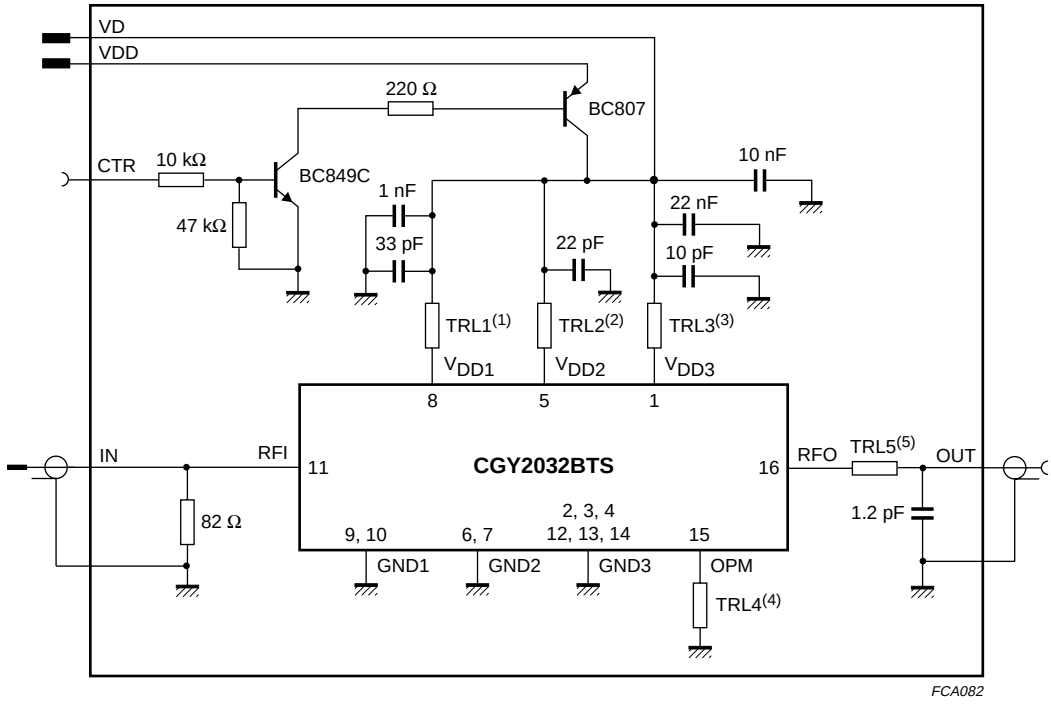


Fig.4 Typical output power and efficiency as a function of supply voltage at P_i = 0 dBm.

APPLICATION INFORMATION

The CGY2032BTS is operated and tested in accordance with the circuit diagram shown in Fig.5. Supply voltage switching is achieved by a single bipolar PNP transistor.



Thickness: 0.8 mm; substrate: FR4; ε_r = 4.7.

(1) TRL1: width = 500 μm; length = 10 mm.

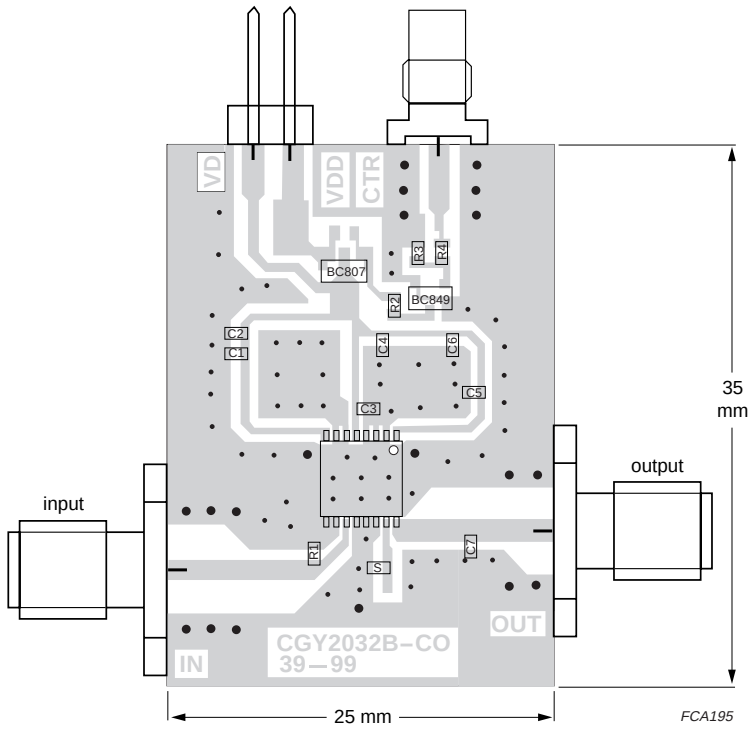
(2) TRL2: width = 500 μm; length = 1 mm.

(3) TRL3: width = 500 μm; length = 8 mm.

(4) TRL4: width = 500 μm; length = 1 to 3 mm; shunt to be adjusted for optimum matching.

(5) TRL5: width = 1400 μm; length = 4.5 mm.

Fig.5 Evaluation board circuit diagram.



See Table 1 for the values of the components.

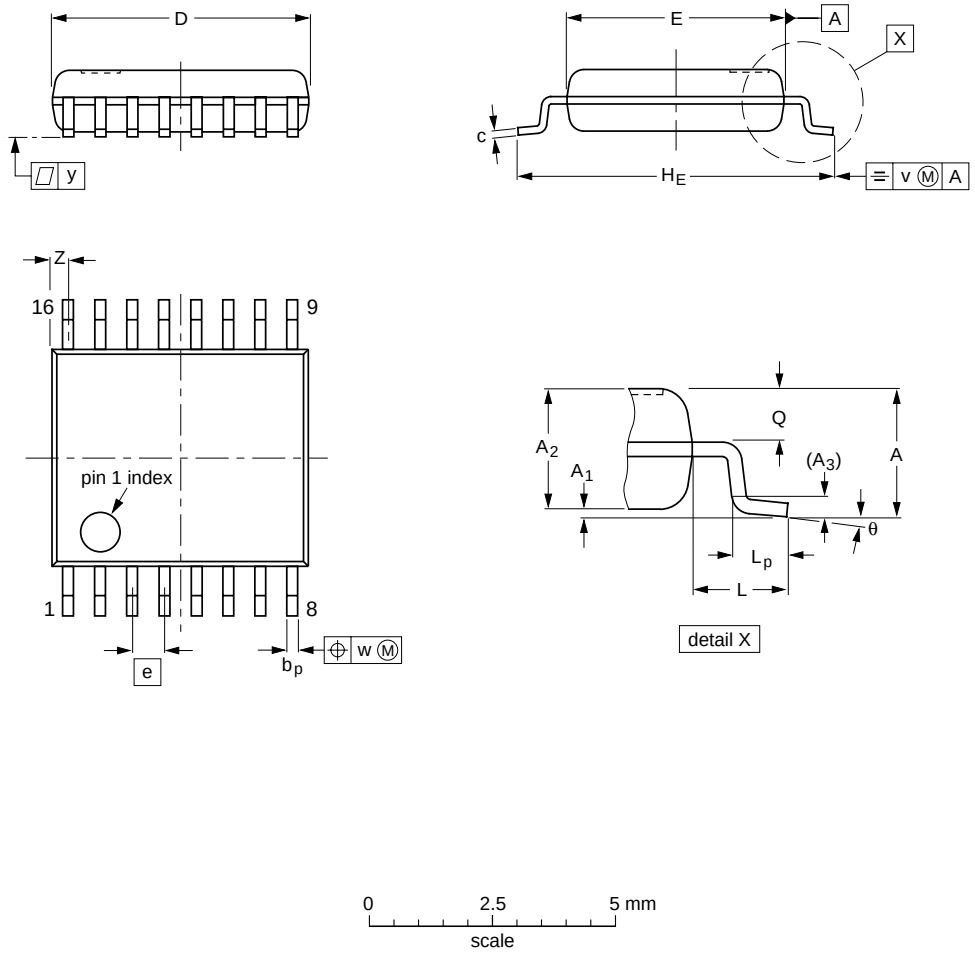
Fig.6 Evaluation board layout.

Table 1 Components list

COMPONENT	VALUE
R1	82 Ω
R2	220 Ω
R3	47 kΩ
R4	10 kΩ
S	shunt
C1	33 pF
C2	1 nF
C3	22 pF
C4	10 nF
C5	10 pF
C6	22 nF
C7	1.2 pF

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1		MO-152				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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